DEVELOPMENT OF A LOW-COST DIGITAL LOGIC TRAINING MODULE FOR STUDENTS LABORATORY EXPERIMENTS

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ABSTRACT

Digital systems have become widely spread, and commonly applicable recently in most of our domestic and office devices like computers, portable digital devices, mobile phones, television, air conditioning, most of industrial machines and motor vehicles. A low-cost digital logic training module for the student's laboratory experiment was designed and realized to simplify the problems of the learner in the study courses like basic electronics, digital logic systems, and computer architecture and so on. The primary goal of this paper was to describe the development and application of an inexpensive digital logic training module prototyping, for hands-on laboratory students' experimentation and research improvement. The duty circle waveform timing sequence for the Digital Logic Training Module (DLTM) was calculated as D, which gives an approximately result of 0.5 seconds. This gives an insight to any students or researcher interested in the development of an economical logic trainer module or related embedded system development. The system features gives advantages of learn-while-doing to compensate the students theoretical knowledge, assist researcher to validate the logical proof and circuit design in the practical exercise related to the basic and derive logic gates (BDLG), combinational logic circuit (CLC) and sequential logic circuit (SLC).

KEYWORDS*: Combinational logic circuit; digital system; hands-on laboratory; industrial machine; learn-while-doing and logic training module*

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1.0 INTRODUCTION

The world over the times has made considerable advancement in digital computerization which is employed in households, industries, commercial and educational sectors. It is realized that the ever growing concentration of modern digital devices and electronics system put innovation and strict requirements on the education, particularly in the field of science technology and engineering (Calazans & Moraes, 2001). A digital logic training system is a command equipment in electronics and digital learning aid which was designed to educate students in the study of logic design skills, practice, testing and modify the digital circuits of the simple network. Digital logic is the processing of only two output states or conditions of ON (1) and OFF (0) with varies number of inputs which can be 2, 3, 4 and so on. The basic and derive logic gates are AND, OR, NAND, NOR, EXOR and EXNOR. The combinational logic circuits are half adder (HF), full adder (FH), multiplexer, decoder etc. While, the sequential logic circuits are flip-flops logic circuit like (S-R, J-K, D and T) which they are incorporated with memory element. This makes output not to depend only on the present input state but also on the past history of input signal. These digital gates are explained and the combinations of these simple gates in various configurations permit more complex logic or counting and mathematics to be computed.

Basic electronic and the digital logic system, are essential courses offered by the students of higher learning in the areas, like computer science and engineering, electrical and electronics engineering and other related fields which was identified as major in their curriculum development (Sothong & Chayratsami, 2010). Of course, the electrical and electronic engineers' experts are professionally aware of the objective of designing digital logic circuits, like clock allocation problems and timing controls, compare to their counterpart in the profession of computer science and engineering who are earlier familiar with digital system in their study. Because, the abstract models from the Boolean algebra expression was used as a basis, as an alternative of circuit theory representation.

The implementation of a universal, low-cost DLTM for students laboratory experiment, in a single module with some functions like a basic and derive logic

gate (BDLG), combinational logic circuit (CLC), and sequential logic circuit (SLC) requires extensive understanding, and also being creative. This can be careful considered as a discrete optimization setback in the logic system based on the opinion of (Manfrini, Helio & Bermadino, 2014). Alba, Luque, Coello and Luna, 2007 claimed that BLG, CLC and SLC design are based on the truth table data that highlight all possible combinations of input variables or logic levels with the equivalent output logic. A truth table of any logic circuit can be given to identify the logic that meets all the conditions provided in the truth table by using traditional techniques or meta-heuristics (Coello, Christiansen & Aguirre, 2000). Since the global optimum for the lowest cost circuit is not stated for some of logic functions, then using meta-heuristics, hybrid particle swarm optimization and differential evolution are suitable for digital circuit designing, flexible and make fault isolation easy to perform (Moore & Venayagamoorthy, 2006). Although, the design of CLCs and others related circuits was stated by (Aguirre and Coello, 2004), that the size of the exploration space grows rapidly as the number of variable input to the circuit increases. This shows that some of the limitations imposed by the truth table must be satisfied to consider the problem of a large number of hard parity restriction.

However, (Carpinelli and Jaramillo, 2001; Jelemenská, 2012) contributed that the challenges remain constant in teaching digital logic system and other related course effectively without experimental activities carried out in the laboratory or learn-while-doing completely involved with the students. One of the proven approaches to facilitate practical skills and experiences is "learning by doing" approach, by undertaking several hands-on laboratory experimentg which allow students to acquire more knowledge and find out the way basic concepts are employed for each case was summarized in the paper of Ajao et al. (2016) and Alasdoon (2013).

Areibi (2001) described boolean algebra as a fundamental area in digital electronics that simplify the logic variable expressions, and analyze the both combinational and sequential logic design. Digits or bits (0 and 1) are widely used in binary coding techniques to code the elements belongs to an information set. For instance, given n to represent the number of bits in the code expression and x represent the number of unique words.

Case 1: Let,
$n = 1$, $x = 2$ then $x^n = 21 = 2$. We have possible input of (0, 1).
Case 2: If,
$n = 2$, x = 2 then $x^n = 2^2 = 4$. We have possible combination input of (00, 01, 10, 11).
Case 3: If
$n = 3$, x = 2 then $x^n = 2^3 = 8$. We have possible combination input of (000,001,010 011,100,101,110 & 111).
Case 4: If
$n = 4$, $x = 2$ *then* $x^n = 2^4 = 16$. We have possible combination input of (0000, 0001, 0010, 0011, 0100, 0101, 0110, 0111, 1000, 1001, 1010, 1011, 1100, 1101, 1110 &111).

Let the number of bit n is given as n = j, while the number of unique words x is given as x = 2j.

Therefore, we can conclude that if elements of information is given to code into the binary coded format, then we have; x < 2j, or j > log2x > 3.32 log10x. Where j, is the number of bits given in a coded word.

The objectives of this paper explained the technologies behind the development and application of a low-cost digital logic training module for the student's laboratory experiment. The system was tested and the result was presented in a truth table. This design is capable of handling the practical exercises of the student, where digital logic fundamental, digital electronic courses and others are offered. It is more useful for the academic research and the developers. Therefore, a digital logic training module will facilitate the level of understanding and familiarization of students with most systems that are digital and logical in nature. Also, it will improve the learning concept, experiment skills in digital electronic techniques and logic circuit design with Boolean expression.

A few attributes possess by DLTM model that give advantage over the preceding design are:

- Compact and easy to operate.
- Dual powered source; AC and DC.
- Additional of learning bread board to verify the electronics component performances.

- Single module with multi-functional circuit.
- Improved fault identification and fault isolation of any defective components.

Students can see and feel the circuit board by touching and familiar with electronic components.

2.0 RELATED WORK

Hacker (2009) designed a low cost student constructed digital trainer. The module was developed to assist the student undertaken digital logic and basic electronics courses to perform and replicate the digital experimental exercise at home using a technology called PortBuffer. The system was inexpensive and portable, but the module is a software simulation based functioning; its operations depend on computer application and could not perform SLC and other tasks. An effort on microcontroller-based real time emulator for logic gate and structured logic devices was presented by (Godwin, Inyiama, Chidiebele & Ekene, 2013). The aim of the author was to find a way out to make the microcontroller become a convenient substitute for any digital device that is readily unavailable for use in the logic design. A system emulator was suggested to take the advantages of digital logic design which can lead to offer of low cost laboratory equipments for efficient skills transfer in the educational systems. The design for SLC is more difficult task than CLC because of the feedback part and redundant states in sequential logic circuits. A module-level Evolvable Hardware (EHW) approach to design synchronous sequential logic circuits was presented by (Tao, Cao, Zhang, Lin & Li, 2012). Genetic Algorithm (GA) was used to minimize the circuit complexity, number of logic gates, wires attached, and obtain near-optimal state assignment. Therefore, sequence detectors, modulo counters, and ISCAS'89 circuit are used as the proof for the simulation evolutionary design approach. Also, genetic algorithm (GA) was used to design combinational logic circuits (CLCs) in the optimization of combinational logic circuits through decomposition of truth tables and evolution of sub-circuits presented in (Manfrini et al., 2014). The goal of the author is to minimize the number of logic elements in the circuit, by proposing a new coding for circuits using a multiplexer (MUX) at the output of the circuit.

With reverence to the author's contribution in the area of digital electronic and logic circuit as review in this paper. Our proposed developed system and illustrations attempts to put into the practices all the techniques, proof from the review paper about the circuit optimization, circuit complexity and minimization. This work makes apparent practicality by developed a low-cost digital logic training module for student laboratory experiment. The approach of "learn-while doing" on the digital electronics, logic circuit design and embedded system projects will help students connect their reasoning from theoretical background to the practical development (Ajao, Olaniyi, Kolo & Ajao, 2015).

3.0 METHODOLOGY

A flexible, user friendly, and self contained low cost digital logic training module was designed and achieved with the use of numbers of integrated circuit (IC) electronic components in the module. The followings are the components wired together to realize the system. A digital complementary metal-oxide semiconductor integrated circuits (CMOSICs), counter, decoder, 7-segment LED display, connector cord, printed circuit board and others.

The system was designed with a switched-mode power supply (SMPS) techniques, using a switching regulator to convert electrical power from 220/240VAC to 12VDC, which gives the advantage of powering the system alternatively with a 9VDC battery. The regulated power unit consists of (IN4001) diode, (470μf, 1000μf/16volt) capacitor and (LM317) regulator.

The output of the gates was configured with OP-Amp in which non-inverting leg was given relevant voltages and inverting legs were made as inputs from the output of the gates and OP-Amp is connected to the LEDs (Light Emitting Diodes). All the gates involved in this circuit received electrical signal from the switches as their input signal, and provide output based on the condition of the switch either in 1 or 0 positions. Pin 14 of the CD4081 was used as an *AND* gate, it is connected to 12VDC, where pin 7 was connected to ground, pin1 and pin2 behaved as input signal, while pin2 behaved as output as depicted in the Figure 12. As a result of this, the same connection was used for all other gates

like CD4070 (EX-OR), CD4069 (NOT GATE), CD4032 (OR GATE), CD4009 (NOR GATE), CD4011 (NAND GATE), and CD4065 (EX-NOR GATE). From this connections and the described configuration, it makes it easy to perform any experiments related to the different categories of BLG, DLG, some CLC like the half adder and full adder logic circuit, and SLC gates. The sequential logic circuit subsystem consists of simple D, T, R-S and J-K flip-flop, which clocked by a free-running or a stable multivibrator. The D flip flop was realized using 74LS74TTL IC and The J-K Flip flop was realized using the 74LS107 TTL IC. The subsystem circuit design of CLC and SLC diagram are shown in the Figure 1 and 2 respectively.

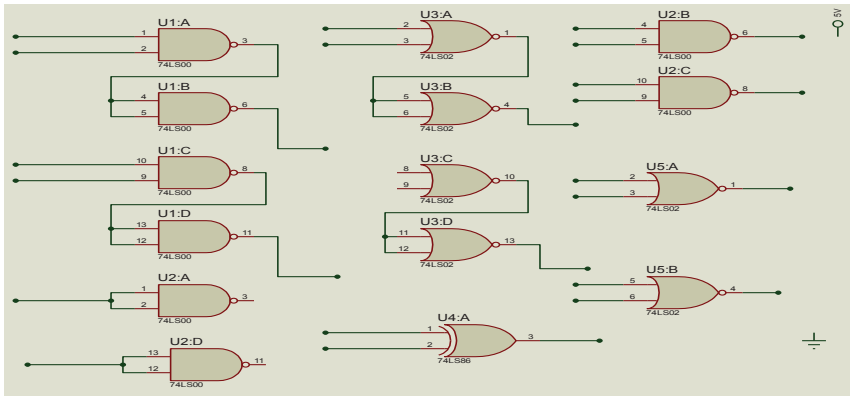

Figure 1. Combinational logic circuit connections.

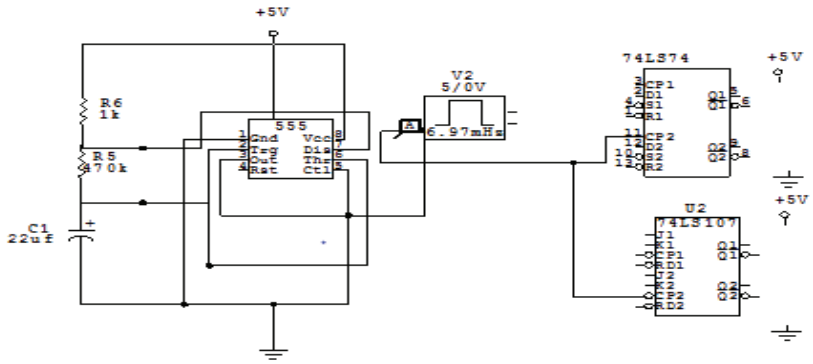

Figure 2. Sequential logic circuit connection with 555 IC timer.

4.0 SYSTEM DEVELOPMENT

4.1 Power Supply Units

This unit consists of a transformer which is used to step down the 220-240AC voltage, IN4007 diodes used to form a bridge rectifier to convert AC to DC, capacitor 1000uF which used as a filter circuit and smoothening, LM317 regulator was used to obtain a +12VDC output regulated value, 330Ω resistor was used to limiting the current flow to the load, and LED was used as indicator light.

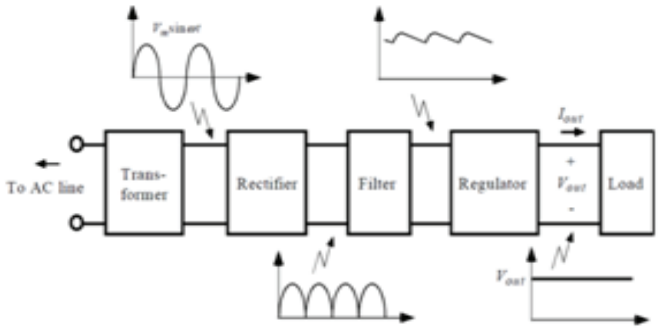

Figure 3. Block diagram of a regulated power supply unit with sinusoidal signal.

4.2 Input Logic Circuit

The input logic circuit provides two logic states, logic 1 defined as voltage level high (usually +5 V) and the logic 0 defined as voltage level low denote (0 V). Figure 2 illustrates details connections of input logic in the system design.

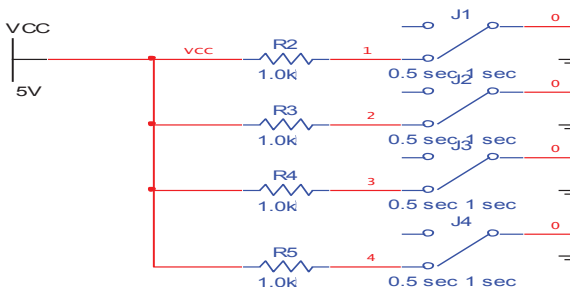

Figure 4. Input time delay logic circuit

4.3 Integrated Circuit 555 Timers and Pulse Generator

The 555 IC timers, an integrated circuit (chip) that is applicable for the variety of timer, pulse generator and oscillator usefulness. The 555 was used to provide time delays, as an oscillator and to a flip-flop element in the design. The design of a flip flops chosen required the application of appropriate clock signals or pulses. This was achieved using the 555 timer IC configured in astable mode. While, the **pulse generator** is a piece of electronic that analyze equipment used to generate rectangular pulses as depicted in the Figure 5.

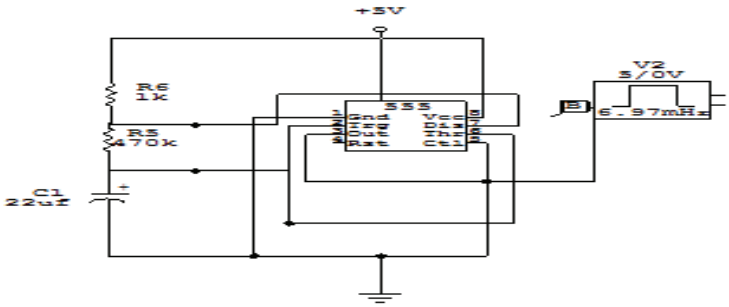

Figure 5. Pulse generator circuit connected with 555 IC timers

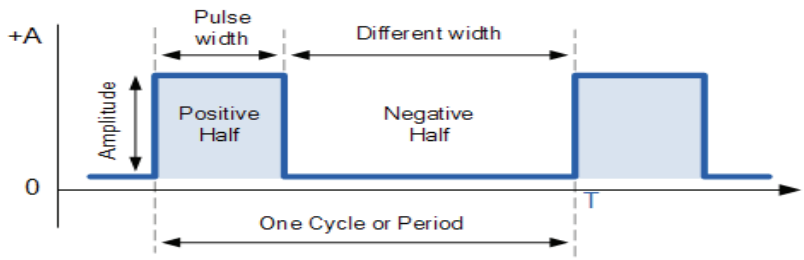

Figure 6. Rectangular waveform of two pulse widths that are unequal time period

Thus, the chosen duty cycle can be calculated from the given Figure 5:

$$T1 = 0.697x(R6 + R5)xC \quad (1)$$

$$T1 = 0.697x(1000 + 470000)x22x10^{-6}$$

$$T1 = 7.2223\ s$$

The discharge time T2 (Output low) is given as:

$$T2 = 0.697x(R5)xC \quad (2)$$

$$T2 = 0.697x(470000)x22x10^{-6}$$

$$T2 = 7.20698\ s$$

The total time for one cycle is given as:

$$T_{total} = (T1 + T2) \quad (3)$$

$$T_{total} = (7.2223 + 7.20698)$$

$$T_{total} = 14.4293\ s$$

The frequency f of one cycle can be calculated as:

$$F = 1/T\ (\text{Hz}) \quad (4)$$

$$F = 1/14.4293$$

$$F = 0.0693\ Hz$$

The duty cycle D is calculated as:

D = Time (output low)/Total time

$$D = T2/(T1 + T2) \quad (5)$$

$$D = 7.20698 / 14.4293$$

$$D = 0.4995\ s$$

4.4 Decoder with 7-Segment display

4.4.1 Decoder

A decoder is a type of combinational logic circuit, which was designed and connected to the common cathode 7-segment display to convert a binary or BCD (Binary Coded Decimal) number to the corresponding decimal value. This can be achieved using 4-inputs (W, X, Y, Z) and a 7- segment display output as (a, b, c, d, e, f, g) as shown in the Figure 7 and the simulation block diagram was depicted in Figure 8. Also, waveform signal for timing analysis is depicted in the Figure 8, after the logic circuit connection for the decoder with 7-segment display was designed and simulated in the Xilins ISE design software.

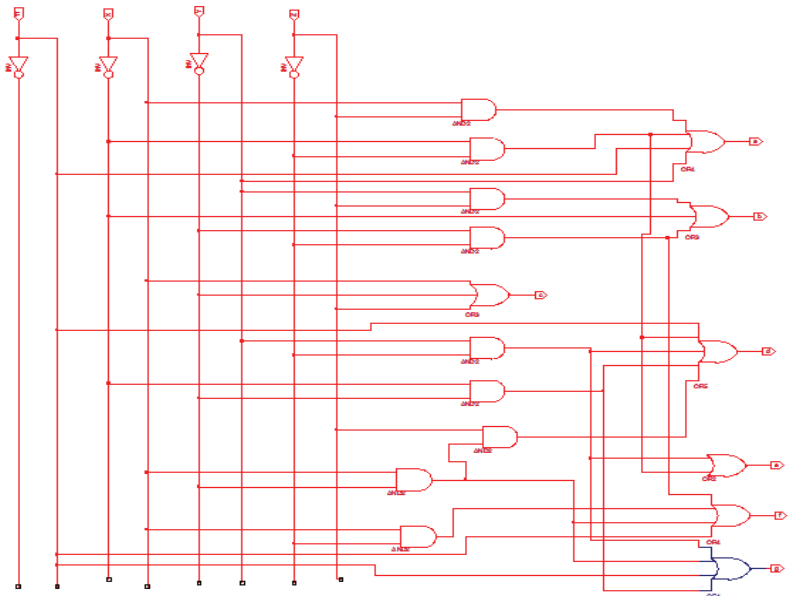

Figure 7. A combinational logic circuit for decoder and 7-segment display

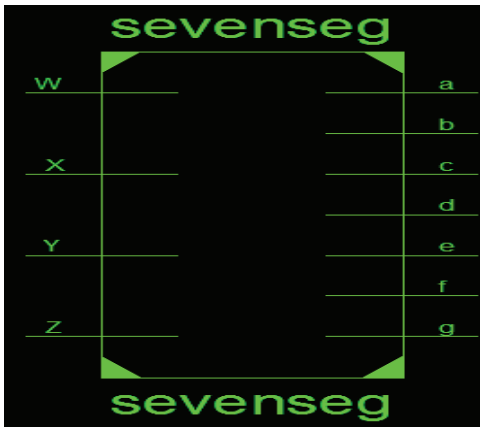

Figure 8. Simulation of block diagram of decoder and 7- segment display

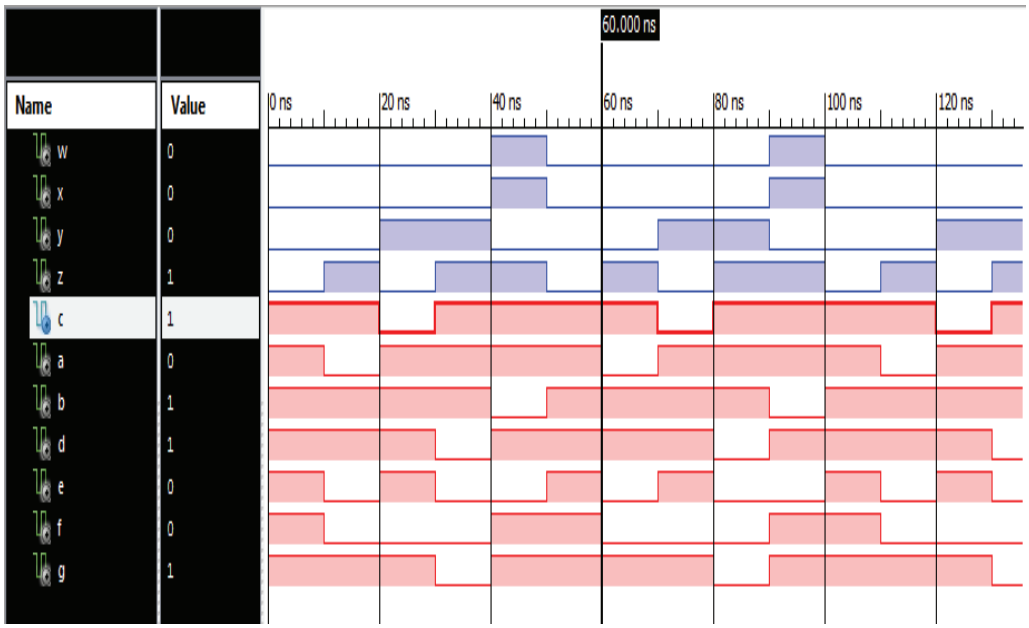

Figure 9. Waveform timing sequence for the decoder with 7- segment display

4.4.2 A 7-segment LED Display

Eight numbers of LED were arranged in a digit form and labeled as 'a' to 'g' to count and display the decimal value from 0-9 using common cathode connections. A common cathode 7 segment display consists of (8 pins and 7 input pins) labeled from '**a**' to '**g**' and the 8th pin is identified as a common ground pin or decimal point (dp) as shown in the Figure 8.

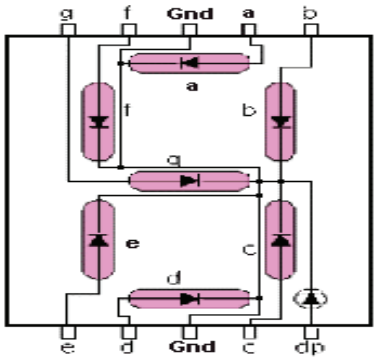

Figure 10. Common cathode connection of 7-segment display (7-segment-led-display-decoder-circuit, 2014)

The 14-pin 7490 counter chip and the 16-pin decoder chip were connected together to drive 7-segment LED displays. A lower voltage supply is used for the cathode connection, which is between 2-3V. The negative side of power is connected to the cathode of each segment of LED display and a high voltage (1) on the segment anode lights up the segment as analyzed in the Table 1 and the output boolean expression for each decimal value's display was given in the Table 2.

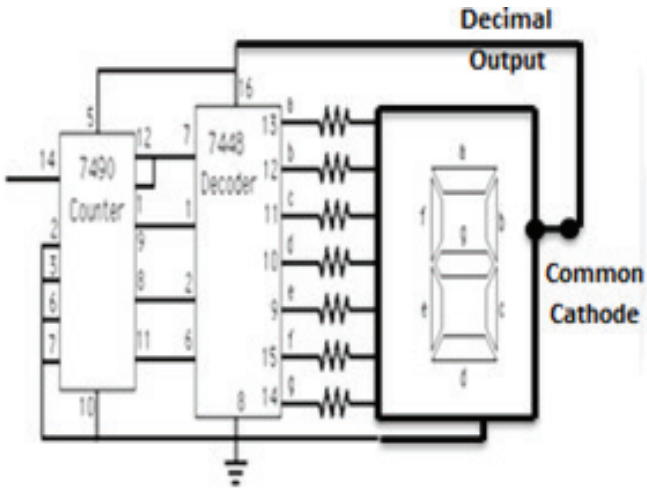

Figure 11. 7-Segment display decoder logic connection

The value of each resistor in the Figure 9 can be calculated as given below;

$$R = V_{cc} - V_f / I_f \quad (6)$$

where R = Series resistor; V_{cc} = 3v, Voltage supply; V_f = 0.7v is barrier potential across the diode and I_f = 10mA is the sink current.

Therefore,

$$R = \frac{3 - 0.7}{10 \text{ x } 10^{-3}}$$

R= 230 Ω

Table 1. Truth Table for Binary Counter (0-9) with seven-segment LED Display using common cathode connection

4-Input Variables				*LED CONNECTION*								*Hexadecimal Value*
W	X	Y	Z	a	b	c	d	e	f	g	dp	
0	0	0	0	1	1	1	1	1	1	0	1	**0**
0	0	0	1	0	1	1	0	0	0	0	1	**1**
0	0	1	0	1	1	0	1	1	0	1	1	**2**
0	0	1	1	1	1	1	1	0	0	1	1	**3**
0	1	0	0	0	1	1	0	0	1	1	1	**4**
0	1	0	1	1	0	1	1	0	1	1	1	**5**
0	1	1	0	0	0	1	1	1	1	1	1	**6**
0	1	1	1	1	1	1	0	0	0	0	1	**7**
1	0	0	0	1	1	1	1	1	1	1	1	**8**
1	0	0	1	1	1	1	0	0	1	1	1	**9**

After using the karnauph map to simplify the expression of the truth table in Table 1, the Boolean expression for the output of LED connection for each decimal value inputted was summariszd in the Table 2.

Table 2. Boolean expression for the output of each LED connection.

S/N	Boolean Expression for Output LED Connection
1.	$a = W + Y + XZ + \bar{X}\bar{Z}$
2.	$b = \bar{X} + \bar{Y}Z + YZ$
3.	$c = X + \bar{Y} + Z$
4.	$d = \bar{X}\bar{Z} + Y\bar{Z} + X\bar{Y}Z + \bar{X}Y + W$
5.	$e = \bar{X}\bar{Z} + Y\bar{Z}$
6.	$f = W + \bar{Y}\bar{Z} + X\bar{Y} + X\bar{Z}$
7.	$g = \bar{X}Y + Y\bar{Z} + X\bar{Y} + X\bar{Y} + W$

5.0 SYSTEM DEVELOPMENT

The development of a low-cost digital logic training module for students' laboratory experiment was designed and illustrated in this paper. The system consists of the digitized module, the board of learning, 7400LS series IC, CMOS CD40 series IC, connector cord, 7490 counter IC, 74LS48 BCD to 7-Segment Decoder IC, 7-segment LED display, AC and DC power supply unit and switches. The block diagram and the logic circuit connection of the design are depicted in the Figure 10 and 11 respectively. Finally, Figure 12 exhibit the snapshort implementation of a working low cost DLTM for the students laboratory experiments.

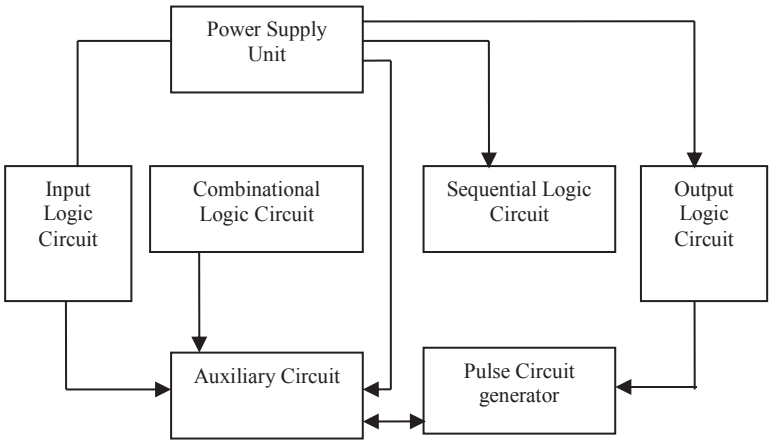

Figure 12. Block Diagram of a digital logic training module

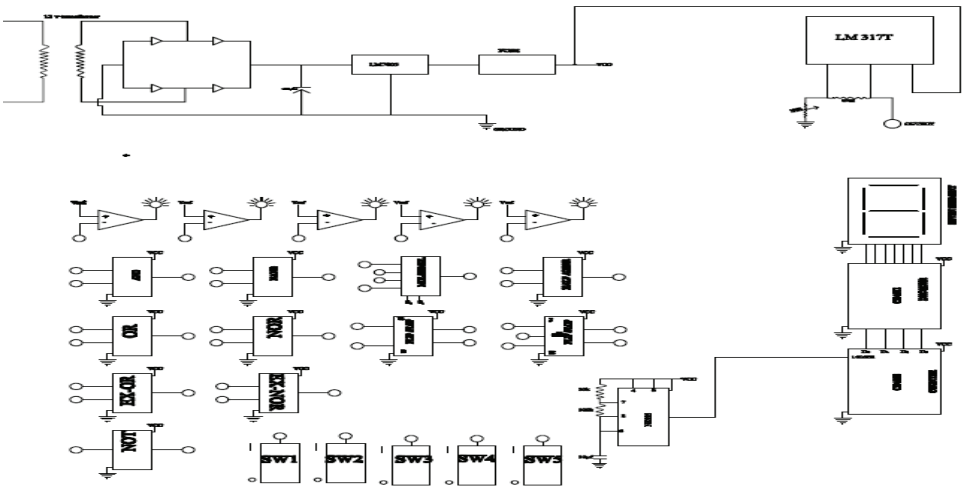

Figure13. Circuit diagram of a digital logic training system

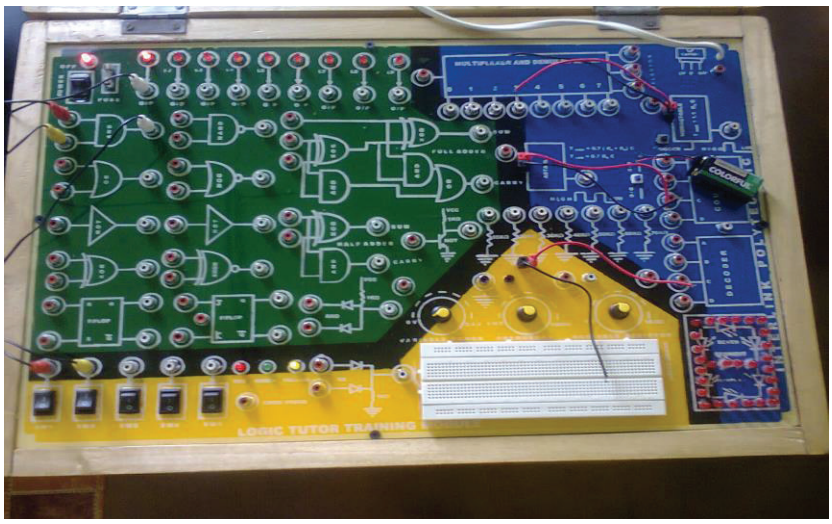

Figure 14. Snapshort of a working low cost of digital logic training module.

6.0 COMPARATIVE STUDY WITH SIMILAR WORK IN THE REVIEW LITERATURE

Different Logic Gates Circuit Trainer were available in the market, they have been studied and analyzed in term of features, functions and cost to ensure the low cost production of proposed digital logic training module for student laboratory experiments. Therefore, most of the integrated circuit (IC) chips and other components used in this designed were relatively available in the market and found cheaper. After the training module was designed, Bills of Engineering Measurement and Evaluation (BEME) was carried out to ensure the actual cost of the students laboratory digital logic training module developed, which is about 50 USD for one DLTM. Table 3 gives comparative cost analysis of the existing logic trainer and the proposed DLTM.

Table 3. Comparative cost analysis of different logic gates trainer module

S/N	Name	Functions	Cost($)
1.	Basic Logic Gates Trainer	Capable of performing only basic logic gates laboratory experiment	40USD
2.	Half and Full adder Trainer Kit	Used for combinational logic circuit experiments like adders and subtractor	40USD
3.	4x4 Bit Binary Multiplier Trainer	Used for only binary multiplier experiments	40USD
4.	General Purpose Logic Gate Trainer	Efficient to perform a lot of experiment on digital logic end electronics	120 USD and above
5.	Proposed Digital Logic Training Module	Efficient to perform the followings experiments; * BLG, CLG and SLG * Multiplexer and Demultiplexer * 7-segment display counter and decoder etc.	50USD

7.0 CONCLUSION

A low-cost digital logic training module for the student's laboratory experiment was developed and packaged in a single module to minimize the cost, and easy to operate by every student. This module is widely applied in the laboratories, where the philosophy and teaching sections can take place over the practical exercise, and research milieu to facilitate the students practical understanding, logic circuit verification and to improve their competency. It will also expose students to the basic electronic theory, digital system and logic principles such as power regulation, ripple filtering, multivibrator, BLG, CLC and SLC. The system prototype worked according to the specification and is quite satisfactory. The "reliability" of the training module developed in terms of response and performance is highly commendable, consistent and easy to operate, and the result of choosing duty cycle of the logic gate per clock/ pulse is given as 0.4995 seconds. Mass productions could be turned out from this design prototype to lower the production costs about USD 50. Therefore, more sophisticated and economical electronic and digital logic training module could be developed using microcontroller chip, field programmable gate array and others to design student laboratory equipment for the digital logic training module. Also, different techniques can as well used in the logic gate designed for the optimization performances and minimization of complex circuitry using Genetic Algorithm, Particle Swarm Optimization and others.

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