CHARACTERIZATIONS OF ELECTROMAGNETIC RADIATED EMISSION FROM DIGITAL ELECTRONIC CIRCUITS IN CONDUCTIVE ENCLOSURE

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ABSTRACT

The issue of electromagnetic compatibility compliance is crucial during the design process of digital circuit boards. This is to control the level of electromagnetic radiated emission and the products to function at satisfactory performance. Basically, an electromagnetic wave radiates whenever time varying currents flow in a circuit. Therefore, it is important to understand the basic concepts of the emission and the suitable mitigation techniques. In this paper, radiated emission measurements in a 3-meter semi-anechoic chamber for two cases of a printed circuit board design are presented and discussed. The first circuit is designed without electromagnetic compatibility consideration and the second is circuit design with electromagnetic compatibility best practices. The results show that the emission level is higher than the product standard limits due to the radiation from the circuit board itself and the interfacing cable. The level can be minimized by keeping the areas of power or signal and its return path loops smaller and the use of a short cable. This means, its behavior as efficient radiating antennas are reduced. The reduction of emission level also can be achieved by considering the employment of damping resistor and common mode chokes. Moreover, the employment of shielding enclosure provides the final option in order to achieve electromagnetic compatibility compliance.

***KEYWORDS**: electromagnetic compatibility, digital electronic circuit, electromagnetic radiated emission, emission reduction.*

1.0 INTRODUCTION

Nowadays, electrical and electronic equipments such as a home entertainment system, personals computing devices and communication equipment operate by using digital techniques. Most of them have

a potential in generating excessive electromagnetic emissions that may interfere and degrade the performance of other equipments as well as the transmission process of radio channels. Consequently, electromagnetic compatibility (EMC) requirements have become a crucial part of modern digital design and should be highlighted for the product to have desired functional performance and to control the amount of electromagnetic waves released to the environments. To comply with the EMC requirements, emission level generated by the radiating structure in the circuit should be minimized as much as possible.

Basically, the radiation of electromagnetic wave is due to both or either differential mode (DM) or common mode (CM) currents flow in a circuit. The DM radiation is characterized by DM current flowing on closed loops, while CM radiation is current flowing in interfacing cable that behaves like transmitting antennas (Paul, 2006). This means that, it is important to keep the loop area for signal or power current and its return path trace as small as possible in order to minimize the effectiveness of the antenna structure. Besides that, the length of the interfacing cable carrying the clock signal should be shorter than the wavelength of clock signal frequency is also crucial. Numerous approaches related to emission suppression methods have been reported in the literature (Turesin, 1967), (See, *et.al*., 2006) and (See, *et.al*., 2005). In (Turesin, 1967), the author outlines limited suggestions on EMC guide to minimize the EMC problems. The researchers in (See, *et.al*., 2006) and (See, *et.al*., 2005) have proven experimentally that the printed circuit board (PCB) layout design without EMC considerations failed to meet EMC requirements. A digital circuit with high ground bounce indicates large circuits loop such as power to ground and signal to ground loops. This leads to high differential mode radiation and also causes high common-mode radiation through interfacing cable that has been verified experimentally in (See, *et.al*., 2006) and (See, *et.al*., 2004).

In this paper, the focus is given on radiated emissions from both digital circuit layout and an interfacing cable that carries a 25 MHz clock signal. Some of the emission reduction techniques are applied on the digital circuit such as small loop area of traces routing, power filtering for 25 MHz clock sources, a damping resistor on the output of an oscillator, ferrite bead and bypass capacitor at output port and decoupling capacitors. CM chokes and short unshielded wire are utilized to minimize CM radiation from cable attached to the digital circuit. The impact of using a shielded enclosure will also be presented.

2.0 DIGITAL CIRCUIT DESIGN

The design of a PCB layout with a good EMC design practices is the cost effective measure to control the radiated emission level from a digital electronic product. In an effort to investigate the radiated emission of a digital electronic circuit, five different PCB layouts carrying clock signals of frequencies 25 MHz, 12.2 MHz, 2.5 MHz, 1.25 MHz, 250 kHz and 125 kHz similar to the schematic circuit proposed in (See, *et.al*., 2006) are designed, fabricated and tested. Besides that, the output port is designed for a 25 MHz signal in order to study the emission of cable. Double-sided FR4 board with relative permittivity 4.7 and thickness of 1.6 mm is employed in this study. A 5 volts regulated voltage is used as a supply voltage to a 25 MHz square wave oscillator.

Initially, the PCB layout is designed without EMC consideration. In the first design, the high-frequency signal and 5 volts power supply currents will flow through a long and large return current path back to its sources forming large power to ground and signal to ground loops antennas. The signal trace is routed on top side and the power trace is routed on another side. The second and the next PCB layouts are designed with a good EMC design practices, the return current path of power and signals currents traces are routed in parallel to each other separated with small distances (forming small loop antenna). A small portion of ground plane is applied under the 25 MHz clock signal traces to provide a low impedance alternative path for the high frequency current. In the third design, two power filters consisting of a ferrite bead and capacitor as proposed in (Montrose, 1999) are included at power supply traces of 25 MHz clock signals. The purpose is to prevent high frequency switching noise current from entering the power distribution network of other ICs. Then, some modification on 25 MHz clock signal traces routing with a damping resistor are made for the fourth PCB layout. The fifth PCB layout is designed with an addition trace routing for output port of 25 MHz clock signal in order to study the effect of interfacing cable on radiated emission level. The ferrite bead, bypass and decoupling capacitors are employed in this PCB design.

3.0 EXPERIMENTAL MEASUREMENT

Generally, the most widely used testing facilities for radiated emission is tested at an open area test site (OATS). A 3-meter semi-anechoic chamber (SAC) on the other hand serves as an alternative option for the OATS as it is able to measure radiated emission without the existence

of ambient noise. The radiated emission of digital circuit is measured in the frequency range of 30 MHz to 1 GHz using a 3-meter SAC at horizontal polarization of antenna. Figure 1 and Figure 2 illustrate the schematic diagram of experimental set-up and the position of the antenna and the equipment under test (EUT) for the radiated emission measurements using the 3-meter SAC respectively. In this paper, the peak value of the measurement results are then compared with the radiated emission limit enforced by the EN 55022 class B standard for Information Technology equipment.

The radiated electromagnetic emission measurement is performed for a digital circuit as shown in Table 1.

Table 1 The radiated electromagnetic emission measurement

i	With large both signal and power loop areas (1st design)
ii	With small both signal and power loop areas (2nd design)
iii	As in (b) plus power filtering (3rd design)
iv	As in (c) and new routing of signal trace with a damping resistor at an oscillator output (4th design)
v	As in (d) plus trace routing for output port with a ferrite bead, bypass and decoupling capacitors (5th design)
vi	With the fifth design plus 60 cm unshielded wire
vii	With the fifth design plus 10 cm unshielded wire with two CM chokes
viii	With the first design plus a shielding enclosure
ix	As in (f) plus a shielding enclosure
x	As in (f) plus 3 CM chokes and a shielding enclosure

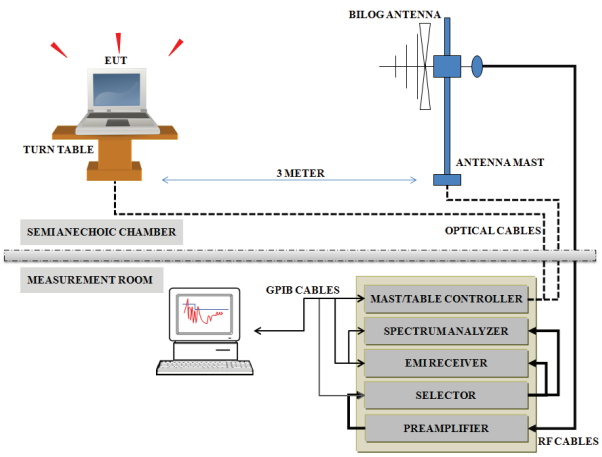

Figure 1 Set-up for radiated emission measurement

Figure 2 Arrangement of BiLog antenna and the EUT

4.0 RESULTS AND DISCUSSION

Experimental measurements are carried out to study the impact of loop area forms by a power or signal and its return current path, the employment of filter on power distribution of the oscillator and integrated circuits switching by 25 MHz clock signal, damping resistor, ferrite bead, bypass and decoupling capacitors, an interfacing cable and shielding enclosure on radiated emission level. In this section, all the measurement results conducted in the 3-meter SAC for the digital circuit operates at various clock frequencies are presented and discussed. It can be seen clearly through the results from Figure 3 to Figure 12, with EMC design practices the digital circuit has complied with the EN 55022 standard. Figure 3 and Figure 4 show the radiated emission levels of the digital circuit design with different routing of return current path of power and signal traces. It can be observed that by routing the power and ground trace in parallel or keeping the loop areas as small as possible, the emission level has reduced significantly especially at frequencies below 500 MHz. The reduction is believed due to the magnetic flux cancellation of DM currents.

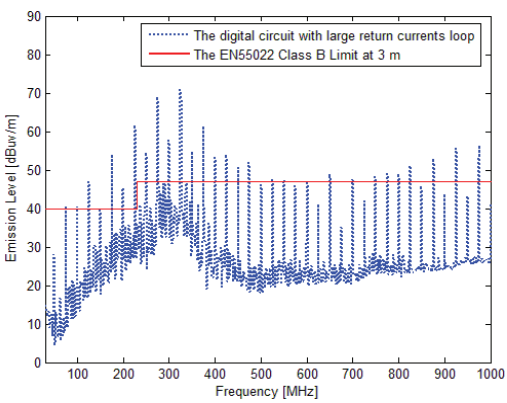

Figure 3 Radiated emission of the PCB design no. 1

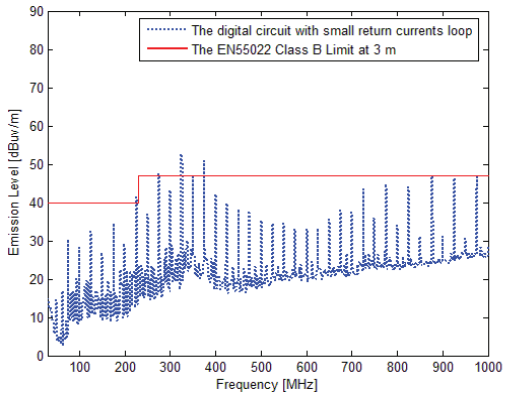

Figure 4 Radiated emission of the PCB design no. 2

Observation of Figure 5 shows that, providing a filtered power for clock signal sources results in a little reduction on the emisson level at the range of frequency from 250 MHz to 350 MHz and 850 MHz to 950 MHz. However, a little increment of emission at frequency of 725 MHz and 775 MHz has been found.

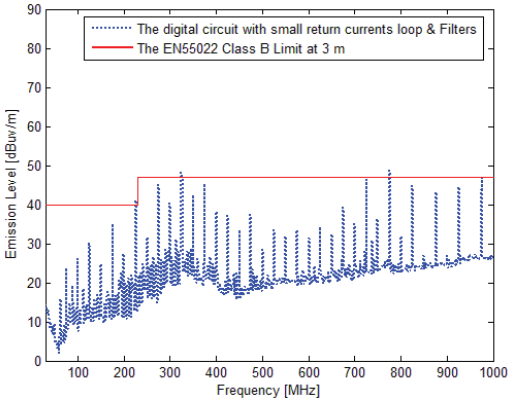

Figure 5 Radiated emission of the PCB design no. 3

Basically, in circuit design, impedance matching is very important to ensure good signal integrity such as no ringing on clock signal due to reflection on the PCB trace. Ringing on clock signal shows that the signal is distorted by high frequency noise which could results high level radiation at high frequency. It can be reduced by using a series damping resistor to match the impedance of sources and the traces. Figures 6 shows that the radiated emissions are reduced when impedance matching is employed.

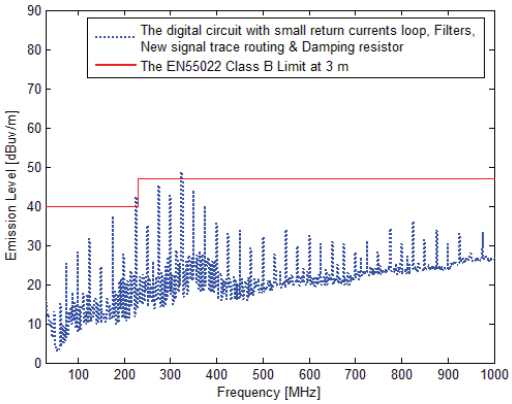

Figure 6 Radiated emission of the PCB design no. 4

Figure 7 shows the radiated emission from the PCB design that has an output port with a combination of EMC practices in a circuit design. The measurement is done with no interfacing cable. It can be observed that the emission levels has met the EN 55022 Class B limit. This means that the digital electronic circuit design with the best EMC design consideration will ensure the circuit to comply with the radiated emission limit.

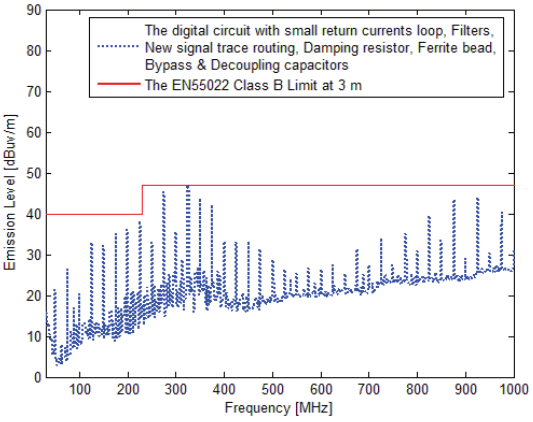

Figure 7 Radiated emission of the PCB design no. 5

However, an introduction of a long unshielded cable attached to output port of the PCB makes the radiated emission of the circuit exceed the emission limit as shown in Figure 8. The increment of the level can be observed at the frequency below 225 MHz, which is about 30 dB and 10 dB at the frequency range around 425 MHz to 800 MHz.

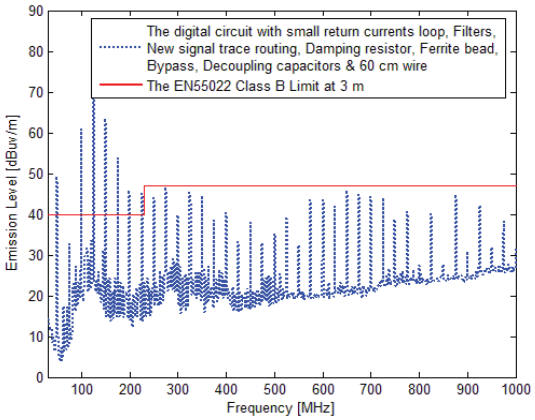

Figure 8 Radiated emission of the PCB design no. 5 with a 60 cm unshielded wire

By reducing the cable length from 60 cm to 10 cm and with the employment of common mode chokes, the emission is reduced significantly and below the EN 55022 Class B limit as shown in Figure 9.

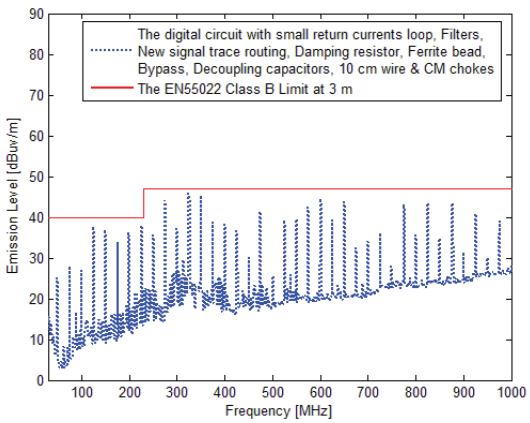

Figure 9 Radiated emission of the PCB design no. 5 with a 10 cm unshielded wire and two CM chokes

Next, experimental measurement is performed to study the effect of shielding enclosure in reduction of radiated emission. The employment of shielding enclosure on poor design PCB could be the final option to further reduce the emission level as shown in Figure 10. However, it will serve no real purpose if unshielded interfacing cable is attached and not grounded to it even the PCB is designed with a good EMC practices. The result can be observed in Figure 11.

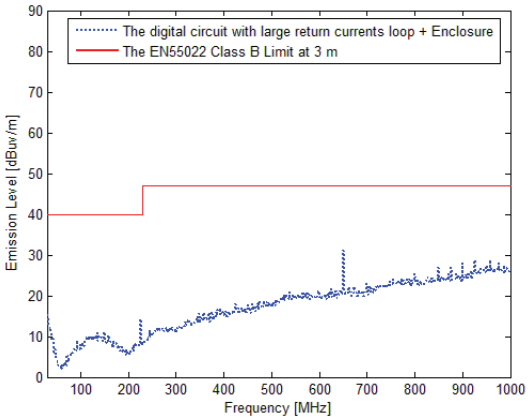

Figure 10 Radiated emission of the PCB design no. 1 in an enclosure

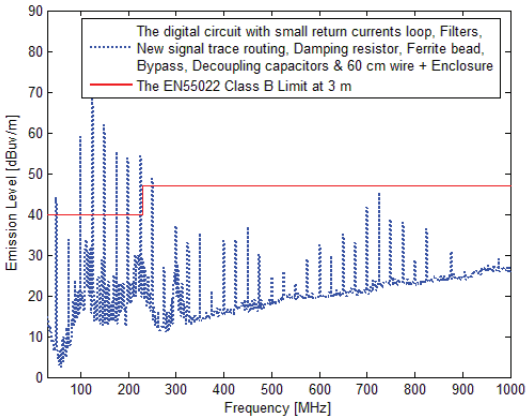

Figure 11 Radiated emission of the PCB design no. 5 with a 60 cm unshielded wire in an enclosure

In order to reduce the emission from the unshielded interfacing cable, the application of CM chokes together with a shielded enclosure is useful as it can reduce the emission level as in Figure 12.

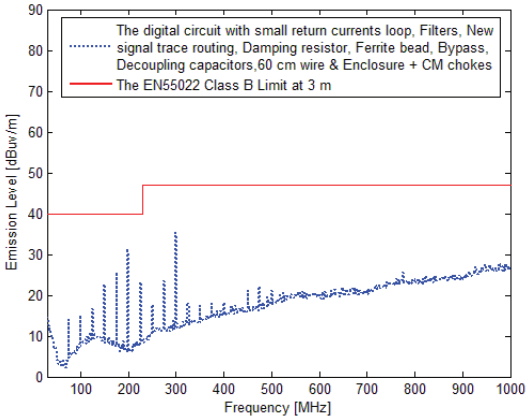

Figure 12 Radiated emission of the PCB design no. 5 with a 60 cm unshielded wire and CM chokes plus an enclosure

5.0 CONCLUSION

Electromagnetic emission level can be minimized with an optimum design of the PCB layout. The results show that, loop area of return current path and cable length have the important impact as unexpected radiating structures. The reduction of emission level can be achieved by keeping the loop smaller and the interfacing cable short. Combination of the different mitigation techniques are required in order to achieve EMC requirements. If a long cable is necessary, CM chokes can be used to minimize the radiation. Moreover, the use of shielding enclosure played an important role as a final option to minimize the emission.

6.0 ACKNOWLEDGEMENT

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