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INVESTIGATION ON OVERCURRENT RELAY SETTING AND PERFORMANCE USING PSCAD SOFTWARE

Mohd Hendra Hairi*[1], Muhammad Nizam Kamarudin[1], Ahmad Sadhiqin Mohd Isira[2], Mohamed Fauzi Packeer Mohamed[3] and Sharizal Ahmad Sobri[4]

[1]Centre for Robotics and Industrial Automation (CeRIA), Faculty of Electrical Engineering, Universiti Teknikal Malaysia Melaka, Hang Tuah Jaya, 76100 Durian Tunggal, Melaka, Malaysia.

[2]Faculty of Electronic and Computer Engineering, Universiti Teknikal Malaysia Melaka, Hang Tuah Jaya, 76100 Durian Tunggal, Melaka, Malaysia.

[3]School of Electrical and Electronic Engineering, Universiti Sains Malaysia, Engineering Campus, Seberang Perai Selatan Nibong Tebal, 14300 Penang, Malaysia.

[4]Faculty of Bioengineering & Technology, Universiti Malaysia Kelantan, City Campus, Pengkalan Chepa, 16100 Kota Bharu Kelantan, Malaysia.

**hendra@utem.edu.my*

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Abstract— This paper presents a study on overcurrent relay setting and performance at 132/33/11kV Hutan Melintang network, Teluk Intan, Perak, Malaysia radial distribution feeder. The study involves an investigation on the existing setting on overcurrent relay and performance. This study includes checking the appropriate relaying Plug Setting (PS) and Time Multiplier Setting (TMS) for the

Overcurrent Relay, Power System, PSCAD	discrimination process. The IEEE std. C37.112 moderately inverse IDMT curve characteristic is chosen for the simulation using the Power System Computer-Aided Design (PSCAD). The result shows that the existing PSM and TMS are well-chosen, and the relay performance is in good condition.

I. Introduction

There are three major components in the electrical power system which is consisting of generation, transmission, and distribution systems. The transmission system links the generators to substations before the supply power reaches the users through the distribution system [1-3]. An electrical power system aims to supply continuous electrical energy to the consumers. As a result, the design must be reliable and economical. It should be able to deliver the energy to a consumer without any interruptions. The system should be protected from power outages and disturbances utilizing a protective relay.

A report has been found that 80% of the interruptions occurred at the consumer side due to the short circuit [4-5]. To make the system reliable and robust from faults, an overcurrent relay is made applicable at the distribution side. Inverse definite minimum time (IDMT) overcurrent relay is widely used as an overcurrent relay device due to its simpleness and economical. The relay operating time is closely related to the current transformer (CT) ratio, plug setting (PS), and time multiplier setting (TMS) [6-7]. However, since the consumer load is expanding over time, reevaluation of the relay setting becomes a necessity.

Analysis of the relay settings had become difficult in old days due to complex mathematical computing. However, it has become more convenient nowadays due to numerous fast and reliable computing methods such as PSCAD MATLAB, ETAP, etc. [8].

This paper presents a study on overcurrent relay setting and performance at 132/33/11 kV Hutan Melintang network, Teluk Intan, Perak, Malaysia radial distribution feeder. The study involves an investigation on the existing setting on overcurrent relay and performance. This study includes checking the appropriate relaying Plug Setting (PS) and Time Multiplier Setting (TMS) for the discrimination process. The IEEE std. C37.112 moderately inverse IDMT curve characteristic is chosen for the simulation using the Power System Computer-Aided Design (PSCAD).

II. Methodology

For power flow analysis, firstly, the single line diagram of Tenaga Nasional Berhad (TNB) Teluk Intan has been reduced to ease the process of modeling in PSCAD software as shown in Figure 1. Then the reduced circuit was used to investigate the performance of the overcurrent relay when subjected to faults.

The load in the circuit model is supplied with 132 kV from the grid through the parallel transformers rated at 132/33 kV and then stepped down at 33/11 kV for both feeders as shown in Figure 1. In the simulation, all the faults were applied at t = 1 sec. The analysis was made by checking on relay tripping time and coordination. Eight cases were studied which involved various types of faults using IEEE std. C37.112 [9] moderately inverse curve. All data were recorded and discussed in the next section.

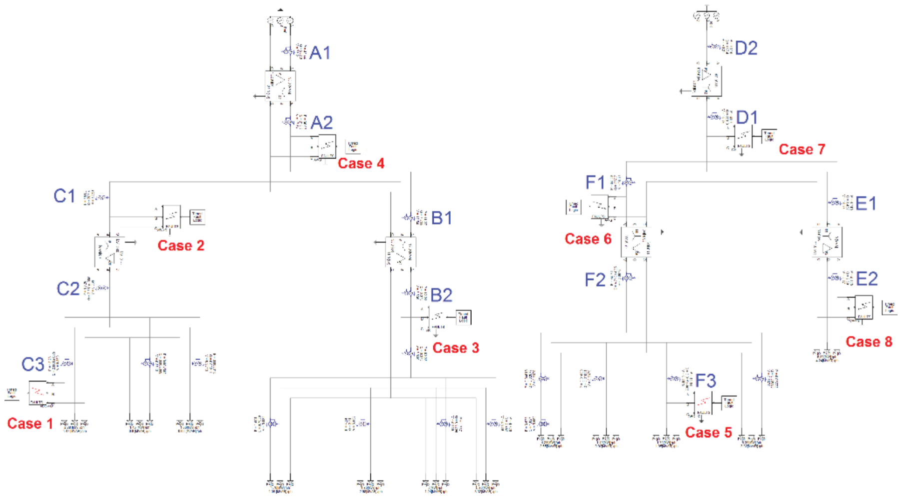

Figure 1: Hutan Melintang Distribution Network Model

To guarantee a reliable, fast, and safe operation of the overcurrent relay, the existing overcurrent relays setting such as pickup current and time dial setting, were carefully investigate. If the existing setting were unsatisfactory chosen, the relay will not properly be functioning or gives the wrong tripping command.

The pickup current of the relays is a function of their rated current, and they are generally ranged from 50% to 200%. In this study, the pickup current for the overcurrent relay as well as the time dial setting is shown in Table 1.

Table 1: Pickup Current and Time Dial Setting

Relay	Rated Current (kA)	Pickup Current (kA)	Time Dial Setting
A1	0.287	0.43	0.59
A2	1.149	1.72	0.44
C1	0.297	0.45	0.47
C2	0.891	1.35	0.24
C3	0.434	0.65	0.01
B1	0.882	1.28	0.30
B2	2.553	3.83	0.12
D1	0.300	0.45	0.78

D2	1.193	1.79	0.59
F1	0.778	1.17	0.48
F2	2.327	3.49	0.26
F3	0.308	0.46	0.08
E1	0.415	0.62	0.63
E2	1.243	1.86	0.41

The value of the pickup current and time dial setting for relay can be determined manually by using the mathematical expression given by [10]. A total of 8 cases were simulated in this study and discussed in the next section.

III. Results and Discussion

The simulations are conducted with 8 different types of faults and locations. The tripping time of the relay when the network is subjected to various faults was observed and recorded.

A. Case 1 (Three-phase-to-ground fault)

There are five relays involves when three-phase faults are applied near the C3 relay which are A1, A2, C1, C2, and C3 respectively as shown in Figure 1. The discrimination times between the relays are 0.2 s. The tripping time for each relay is recorded and analyzed by comparing it with the calculation value as shown in Table 2. The timed fault logic is the time to apply fault.

It can be seen in Table 2 that the calculated (timed fault logic (TFL) + t (s)) and simulation tripping time closely match, which indicates that the relay setting and discrimination are performing well for three-phase faults.

Table 2: The Simulation Time and Calculation Time

Relay	Calculation tripping time, t (s)	Timed Fault Logic (TFL) + t (s)	Relay tripping time simulation (s)
A1	0.82	1.82	1.81
A2	0.61	1.61	1.61
C1	0.41	1.41	1.41
C2	0.21	1.21	1.21
C3	0.01	1.01	1.01

B. Case 2 (Two-phase-to-ground fault)

The two-phase-to-ground fault is applied as shown in Figure 1. The relays tripping time is recorded and shown in Table 3.

It can be seen in Table 3 that the calculated (timed fault logic (TFL) + t (s)) and simulation tripping time closely match, which indicates that the relay setting and discrimination are performing well for double phase faults. The discrimination time between relay C1 and A2 is 0.05 s, while relay A2 and A1 is 0.13 s.

Table 3: The Simulation Time and Calculation Time

Relay	Calculation tripping time, t (s)	Timed Fault Logic (TFL) + t (s)	Relay tripping time simulation (s)
A1	0.41	1.41	1.41
A2	0.29	1.29	1.29
C1	0.24	1.24	1.24

C. Case 3 (Two-phase-line-to-line fault)

The two-phase-line-to-line fault is simulated, and the result is shown in Table 4.

It can be seen in Table 4 that the calculated (timed fault logic (TFL) + t (s)) and simulation tripping time closely match, which indicates that the relay setting and discrimination are performing well for double phase faults. The discrimination time between relay B1 and A2 is 0.11 s.

Table 4: The Simulation Time and Calculation Time

Relay	Calculation tripping time, t (s)	Timed Fault Logic (TFL) + t (s)	Relay tripping time simulation (s)
A1	0.44	1.44	1.44
A2	0.32	1.32	1.32
B1	0.20	1.20	1.21
B2	0.08	1.08	1.09

D. Case 4 (Single-phase-to-ground fault)

The single-phase-to-ground fault is simulated, and the result is shown in Table 5.

It can be seen in Table 5 that the calculated (timed fault logic (TFL) + t (s)) and simulation tripping time closely match, which indicates that the relay setting and discrimination are performing well for single-phase faults. The discrimination time between relay A1 and A2 is 0.12 s.

Table 5: The Simulation Time and Calculation Time

Relay	Calculation tripping time, t (s)	Timed Fault Logic (TFL) + t (s)	Relay tripping time simulation (s)
A1	0.44	1.41	1.41
A2	0.32	1.29	1.29

E. Case 5 (Single-phase-to-ground fault)

The single-phase-to-ground fault is simulated, and the result is shown in Table 6.

It can be seen in Table 6 that the calculated (timed fault logic (TFL) + t (s)) and simulation tripping time closely match, which indicates that the relay setting and discrimination are performing well for single-phase-to-ground fault. The average discrimination time between each relay is 0.2 s.

Table 6: The Simulation Time and Calculation Time

Relay	Calculation tripping time, t (s)	Timed Fault Logic (TFL) + t (s)	Relay tripping time simulation (s)
D1	0.86	1.86	1.86
D2	0.65	1.65	1.65
F1	0.46	1.46	1.45
F2	0.25	1.25	1.25
F3	0.05	1.05	1.05

F. Case 6 (Two-phase-to-ground fault)

The two-phase-to-ground fault is simulated, and the result is shown in Table 7.

It can be seen in Table 7 that the calculated (timed fault logic (TFL) + t (s)) and simulation tripping time closely match, which indicates that the relay setting, and discrimination are performing well for the two-phase-to-ground fault. The discrimination time between each relay range from 0.1 and 0.2 s.

Table 7: The Simulation Time and Calculation Time

Relay	Calculation tripping time, t (s)	Timed Fault Logic (TFL) + t (s)	Relay tripping time simulation (s)
D1	0.57	1.57	1.57
D2	0.39	1.39	1.39
F1	0.29	1.29	1.29

G. Case 7 (Two-phase-line-to-line fault)

The two-phase-line-to-line fault is simulated, and the result is shown in Table 8.

It can be seen in Table 8 that the calculated (timed fault logic (TFL) + t (s)) and simulation tripping time closely match, which indicates that the relay setting and discrimination are performing well for the two-phase-line-to-line fault. The discrimination time between relay D1 and D2 is 0.12 s.

Table 8: The Simulation Time and Calculation Time

Relay	Calculation tripping time, t (s)	Timed Fault Logic (TFL) + t (s)	Relay tripping time simulation (s)
D1	0.52	1.52	1.52
D2	0.40	1.40	1.40

H. Case 8 (Two-phase-to-ground fault)

The two-phase-to-ground fault is simulated, and the result is shown in Table 9.

It can be seen in Table 9 that the calculated (timed fault logic (TFL) + t (s)) and simulation tripping time closely match, which indicates that the relay setting and discrimination are performing well for two-phase-to-ground fault. The discrimination time between relay B1 and A2 is 0.11 s.

Table 9: The Simulation Time and Calculation Time

Relay	Calculation tripping time, t (s)	Timed Fault Logic (TFL) + t (s)	Relay tripping time simulation (s)
D1	1.03	2.03	2.01
D2	0.77	1.77	1.76
E1	0.57	1.57	1.56
E2	0.37	1.37	1.36

IV. Conclusion

The purpose of overcurrent relay protection and coordination is to minimize the damage and isolate the faulty as soon as possible. The discrimination time margin or coordination time between each overcurrent relay is 0.3 s and 0.4 s for electromechanical relays: and from 0.1 s to 0.2 s for microprocessor-based relays [11]. As the relay at Hutan Melintang network is in the form of electromechanical type, it was found that the discrimination time is in the range of 0.3 - 0.4 s which is acceptable. Also from this study, it was found that the existing PS and TMS are considered satisfactory considering the complexity of the network and the uncertainties associated with the type of fault and their locations. The calculation values and the simulation result shows that the tripping time is closely matched with each other.

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