Journal of Engineering and Technology

ISSN 2180-3811 eISSN 2289-814X https://jet.utem.edu.my/jet/index

THERMAL-AWARE TEST SCHEDULING AND FLOOR PLANNING FOR THREE-DIMENSIONAL STACKED INTEGRATED CIRCUITS

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Article history:
Received Date: 5 July 2024
Revised Date: 1 October 2024
Accepted Date: 21 November 2024

Keywords: 3D-SIC, Floor Planning, Test Scheduling, Test Time, Thermal-aware

Abstract— Testing three-dimensional stacked integrated circuits (3D-SICs) remains a challenging task due to the complexity of generating an optimized test schedule that minimizes test time. One of the main challenges is accessing upper dies, which is only possible through the bottom die, requiring the extension of Test Access Mechanisms (TAMs) via Through-Silicon Vias (TSVs). Additionally, the limited number of primary I/O pins, TSVs, and TAM width necessitates efficient resource allocation. Effective thermal management is crucial due to the high-power consumption of cores and uneven power distribution, which pose overheating risks. Advanced

concurrent test scheduling is essential to allocate resources effectively while maintaining power and temperature limits. This research proposes a thermal-aware test scheduling optimization combined with floor planning for 3D-SICs, where the floor planning is computed using a simulated annealing algorithm based on a set of pareto optimal cubes chosen by an Ant Colony Optimization (ACO) algorithm. The subsequent thermal-aware 3D-SIC test scheduling, considering resource and power constraints, is generated using a 3D Bin Packing method. The objective is to minimize test schedule time while considering resource and power constraints. Experimental results using multiple ITC'02 benchmark circuits indicate an average estimated improvement of 0.25% in test schedule efficiency when incorporating floor planning into test scheduling, compared to scheduling without floor planning. These findings underscore the significance of integrating thermal-aware test scheduling with floor planning, highlighting its potential to significantly enhance test efficiency, reduce power consumption, and ensure reliable testing of 3D-SICs under stringent resource and thermal constraints.

I. Introduction

The trend of integrating entire electronic systems onto a single chip is becoming increasingly prominent in today's technology landscape. Although

advancements in integrated circuit (IC) technology have enabled smaller feature sizes, traditional System-on-Chips (2D-ICs) are expanding in width due to the growing demand for semiconductor devices with enhanced functionalities, such as those found in modern smartphones. This expansion, however, presents challenges in circuit performance because lengthy interconnects between cores become the primary bottleneck in 2D-IC designs. To address this, three-dimensional stacked integrated circuit (3D-SIC) technology has emerged, which stacks circuit components into multiple layers with vertical interconnections, known as Thru-Silicon Vias (TSVs). This approach reduces horizontal interconnect lengths and offers improved functionality, increased bandwidth, and a reduced footprint [1-4].

Despite the benefits of 3D-SICs, testing remains a challenge due to the vertically stacked dies. The transmission of test data between the test pins and the cores located on different dies relies on test access mechanisms (TAMs) and TSVs [1]. However, the limited availability of test resources such as test pins, TAMs, and TSVs necessitates an efficient allocation and utilization of these resources. Finding an optimal solution is inherently complex [2-4]. As a result, researchers often use heuristics and approximation algorithms to develop near-optimal test schedules, aiming to minimize the test schedule time effectively [5-7].

Concurrent testing of multiple cores can reduce the test schedule time of a 3D-SIC but increases power consumption, risking system-level power limits and potential core damage [2-4]. Simultaneous testing of adjacent cores with higher power density (hot modules) can create hotspots, which compromise chip reliability [8]. Therefore, researchers often adopt power and thermal-aware test scheduling strategies to manage test concurrency, ensuring that the overall power consumption and temperature of the 3D-SIC remain within system limits [8-9].

The placement of cores within the stack and their test duration significantly impacts heat dissipation capabilities. Cores farther from the heat sink dissipate heat more slowly, regardless of their power consumption. Longer test times generate more heat, exacerbating potential hotspots. Thus, test scheduling must consider core heat dissipation, ensuring sufficient space around cores for heat dissipation to prevent hotspot formation and irreversible damage to the 3D-SIC [8-9].

Heat transfer from hot modules to cooler adjacent cores can help prevent hotspot formation, promoting more test concurrency [11]. However, if hot modules are positioned far from the heat sink, they may dissipate heat less effectively, raising the overall temperature of the 3D-SIC. Ideally, hot modules should be placed closer to the heat sink, often at the top of the stack, but this can increase the need for more TSVs, thus raising costs. Therefore, relying solely on resource, power, and thermal-aware test scheduling is insufficient; thermal-aware floor planning with TAM consideration is crucial for the quality of the test schedule, a factor that previous research has not thoroughly addressed.

II. Methodology

The subsections below outline the methodology employed in this research, including the problem formulation, the proposed research methodology flow, the process of data collection, and the tools and algorithms utilized.

A. Problem Formation

Given a 3D-SIC to be designed with (i) maximum allowable number of stack, (ii) maximum TAM width limit, Wmax, (iii) maximum TSV limit, TSVmax, (iv) number of cores, C*i*, (v) the number of I/O terminals per C*i*, (vi) the number of internal scan chains per C*i*, (vii) the length of each internal scan chains, (viii) the number of test patterns associated with each C*i*, (ix) maximum power limit, Pmax, (x) maximum thermal limit, Tmax, co-optimization of thermal-aware test scheduling

and floor planning technique is performed to obtain a test schedule for 3D-SIC with minimal test time under Pmax, Tmax and resource constraints. The research methodology depicted in Figure 1 guides the co-optimization procedure for thermal-aware test scheduling and floor planning, taking into account resource and power constraints. The primary goal is to develop a test scheduling technique for 3D-SICs that minimizes total test time.

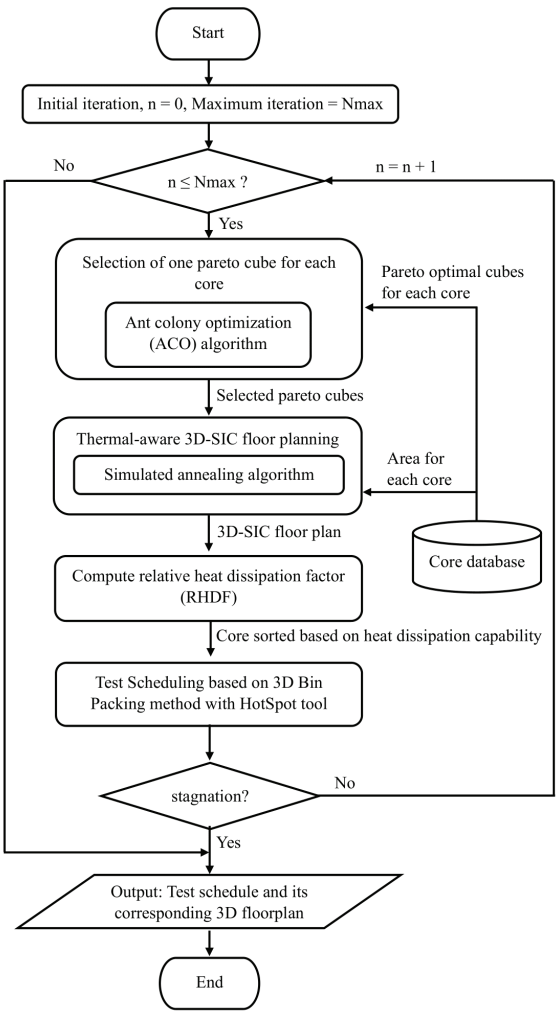

Figure 1: Co-optimization procedure for thermal-aware test scheduling and floor-planning in 3D-SICs

B. Pareto Test Cubes

To facilitate modular testing and optimize the use of TAM widths and core I/O pins, multiple wrapper designs are generated for each core using the Design Wrapper heuristic based on the Best Fit Decreasing (BFD) algorithm, proposed in [12]. The test time for each wrapper design is calculated, resulting in a range of test times for each core across different TAM widths. Pareto optimal points are then identified, and for each point, power consumption is estimated based on the core's global peak power consumption. Each core under a specific pareto optimal wrapper design is represented as a three-dimensional cube, where dimensions correspond to TAM width, power consumption, and test time.

C. Ant Colony Optimization

The Ant Colony Optimization (ACO) algorithm is employed to select Pareto cubes for use in 3D-SIC floor planning and test scheduling. In ACO, each core is denoted as Ci ($1 \leq i \leq N$), where N represents the total number of cores in the 3D-SIC. Each Ci is associated with a set of Pareto optimal cubes (Ri). Each cube (ri) in Ri has dimensions where the height represents the allocated TAM width for the jth wrapper configuration, wij, the width represents the corresponding test time, T(wij), and the third dimension represents the peak power, P(wij).

ACO utilizes both pheromone trail values and heuristic favourability to find solutions. In this study, the heuristic favourability, denoted as Wprefer, signifies the preferred TAM width for Ci. Initially, during generation, the Pareto cube in Ri with the highest TAM width, which corresponds to the lowest test time, is selected as Wprefer for each Ci. Subsequently, Wprefer for each core, Ci, is updated to the corresponding Pareto cube from the set Rglobal of the global best ant, which results in the lowest test schedule time. This approach guides the search and prevents it from becoming overly focused on local optima. The pheromone trail value,

denoted as $\tau(i,j)$, reflects the attractiveness of choosing a Pareto cube with TAM width j for core i [13]. The probability of selecting TAM width j for core i is calculated using Equation (1):

$$\boldsymbol{prob(i,j)} = \frac{[\boldsymbol{\tau(i,j)}]^{\boldsymbol{\alpha}} \cdot \boldsymbol{\beta}}{\sum_{\boldsymbol{j=1}}^{\boldsymbol{W_{max}}}([\boldsymbol{\tau(i,j)}]^{\boldsymbol{\alpha}} \cdot \boldsymbol{\beta})} \quad (1)$$

where:
$Wmax$ = Maximum TAM width
α = Relative importance of $\tau(i,j)$
β = Relative importance of wij

In the ACO algorithm, a predetermined number of ants are initially placed randomly within the test cubes during initialization. Each ant proceeds iteratively to select test cubes for each core. By the end of N-1 iterations (where N is the number of cores), every ant has chosen a test cube for each core. These cubes form the basis for thermal-aware 3D-SIC floor planning, leading to the generation of multiple floorplans. Each floorplan undergoes thermal-aware test scheduling under power and TAM constraints, resulting in various overall test times. The set of cubes that yields the shortest test time is identified as Rglobal, while Rlocal represents the optimal solution discovered during the current iteration of ACO, primarily used to update the pheromone trail. This iterative process continues until either reaching the maximum cycle count or stagnation, characterized by all ants selecting the same cubes with identical test times.

D. Thermal-aware 3D Floor planning

Each ant's chosen set of cubes undergoes thermal-aware floor planning using a simulated annealing algorithm. The objective is to explore various configurations and determine the most optimal floor plan considering thermal factors and TAMs, ultimately minimizing the test schedule time for a 3D-SIC. Input parameters include the number of 3D-SIC layers and the maximum area per layer. Additionally, detailed information for each core, such

as its area (a*i*), power density (p*ij*), and TAM width (w*ij*), is gathered. To identify the hot modules within the 3D-SIC, the average power density (p_avg) of all cores in the set is calculated. Cores with a power density greater than p_avg are designated as hot modules. Hot modules can significantly impact the temperature within the 3D-SIC, while non-hot modules have a lesser effect. To mitigate potential hotspots and manage peak temperatures, special attention is given to strategically placing the hot module in its designated position [11].

In this study, optimal placement of the hot module involves several critical considerations. Firstly, it's crucial to avoid clustering hot modules together to prevent localized temperature build-up. Secondly, positioning the hot module closer to the heat sink is advantageous for efficient heat dissipation, thereby maintaining temperatures within acceptable limits. Lastly, placing the hot module at the edge of the layer can enhance heat dissipation by maximizing exposure to ambient air. Adhering to these guidelines can significantly enhance the overall thermal performance and reliability of the 3D-SIC.

The thermal-aware floorplanning algorithm is summarized as follows: Initially, hot modules are placed optimally based on optimal placement considerations. Subsequently, a random floor plan is then generated by positioning non-hot modules among the hot modules. To address thermal considerations, intra-layer and inter-layer thermal effects are calculated specifically for the hot modules within the floor plan, using methods proposed in [11]. The quality of the floor plan is evaluated using a cost function (CF) described by Equation (2):

$$\boldsymbol{CF} = (\boldsymbol{\xi} * \boldsymbol{x}) + (\boldsymbol{\delta} * \boldsymbol{y}) + (\boldsymbol{\zeta} * \boldsymbol{z}) - (\boldsymbol{\eta} * \boldsymbol{w}) \quad (2)$$

where:
ξ = Relative importance of TSV count
x = TSV
δ = Relative importance of area
y = Area

ζ = Relative importance of inter-layer heat
z = Inter-layer heat
η = Relative importance of intra-layer heat
w = Intra-layer heat

This function integrates factors such as TSV count, power distribution, and thermal effects to provide a quantitative measure of floor plan quality. A lower cost value indicates a more favourable configuration that balances these considerations. To refine the solution, simulated annealing algorithm was used by performing a series of five perturbation operations: Intralayer swap, Intralayer move, Rotation, Interlayer swap, and Interlayer move. These operations aim to explore alternative configurations that potentially yield lower cost functions. The process of evaluating the cost function and performing perturbation operations iterates until an optimal solution is achieved or the maximum iteration limit is reached.

E. Relative Heat Dissipation Factor

For each ant, various parameters are derived from earlier sections, including the number of layers in the 3D-SIC, maximum layer surface area, thickness of the 3D-SIC, thickness of the thermal interface material (TIM), thickness of the die layer, core placements within the 3D-SIC, core areas, and power trace values. These parameters are utilized to calculate the Relative Heat Dissipation Factor (RHDF) for each core in the 3D-SIC, based on Equation (3):

$$\boldsymbol{RHDF = HHDF * VHDF * PT} \quad (3)$$

where:
HHDF = Horizontal Heat Dissipation Function
RHDF = Vertical Heat Dissipation Function
PT = Power Trace

The HHDF for each core within a layer is determined by measuring its distance from the four edges of the layer on the horizontal plane. This distance

sum represents the core's ability to dissipate heat horizontally. In contrast, the VHDF evaluates the layer's position within the stack relative to the heat sink, measuring how far each layer is from the heat sink to assess vertical heat dissipation. The RHDF for each core is calculated by multiplying the HHDF and VHDF values, providing a metric that reflects the core's heat dissipation capability considering both its horizontal and vertical positions in the stack. Additionally, the RHDF incorporates the core's power trace value and the duration of testing, represented by the number of clock cycles used. This thorough evaluation ensures a precise assessment of each core's heat dissipation efficiency [8].

F. Thermal-aware Test Scheduling

After obtaining a set of cubes from the ACO algorithm and generating the 3D-SIC floorplan, each ant's cores (cubes) are sorted in non-increasing order based on their RHDF values. This sorting ensures that cores with lower heat dissipation capability, which could potentially generate excessive heat during testing, are prioritized during the scheduling process. Subsequently, the 3D bin packing algorithm takes these cubes along with the RHDF list corresponding to each ant, as well as inputs such as the maximum TAM width limit (Wmax), maximum power limit (Pmax), and maximum thermal limit (Tmax). The objective is to optimize the scheduling of these cubes while adhering to constraints: ensuring that the total TAM width usage does not exceed Wmax, the total power consumption remains below Pmax, and the maximum temperature remains below Tmax throughout testing process.

The scheduling process commences by selecting the first cube from the RHDF list and placing it in a 3D bin. Subsequently, the next cube is selected while applying the adjacency exclusion principle. This principle dictates that the next cube can only be scheduled if it is not adjacent to the previously scheduled cube

within the same test session in the 3D-SIC floorplan. This approach ensures adequate space around each tested core for effective heat dissipation, thereby preventing heat accumulation and hotspot formation. If the next cube is found to be adjacent to the previously scheduled core within the same test session, it is temporarily placed in a list to be scheduled in the subsequent test session. Before scheduling the next selected cube, the algorithm checks the availability of unallocated TAM width to determine if test concurrency is feasible. Additionally, the algorithm verifies that scheduling the cube will not exceed the power limit by calculating the cumulative power consumption of all scheduled cores up to that point. Furthermore, the algorithm assesses whether scheduling the cube satisfies the thermal limit by using the HotSpot 6.0 Tool to check the maximum temperature from the beginning to the end of the test session [14]. If the cube satisfies all three constraints (TAM width, power limit, and thermal limit), it is scheduled within the 3D bin. If a cube fails to meet any of these limits, it is placed in the temporary list for scheduling in subsequent test sessions as conditions permit

III. Main Result

To implement and validate the proposed test scheduling and floor planning technique for 3D-SICs, we will utilize the widely recognized ITC'02 SoC benchmark circuits [15]. These benchmarks are established as standard representative designs widely used in integrated circuit testing research. Specifically, core information from four benchmark SOCs will be utilized: d695 (an academic benchmark), as well as industrial SOCs p22810, p34392, and p93791. The parameters for 3D-SIC and thermal considerations will be adopted from [8].

Figure 2 illustrates the thermal-aware floor planning approach using a simulated annealing algorithm, which strategically places hot modules, indicated by red-bordered squares, adjacent to non-hot modules, shown by blue-bordered squares. This

arrangement enhances cooling efficiency by allowing non-hot modules to act as thermal buffers, absorbing and dissipating heat from the hot modules. This configuration prevents localized heat build-up by distributing the thermal load more evenly and mitigating the risk of overheating. Although the algorithm does not guarantee that all hot modules are positioned at the edges of the layers, which could offer optimal exposure to ambient air, it still improves heat dissipation by promoting effective heat transfer to cooler modules and supporting better overall thermal management.

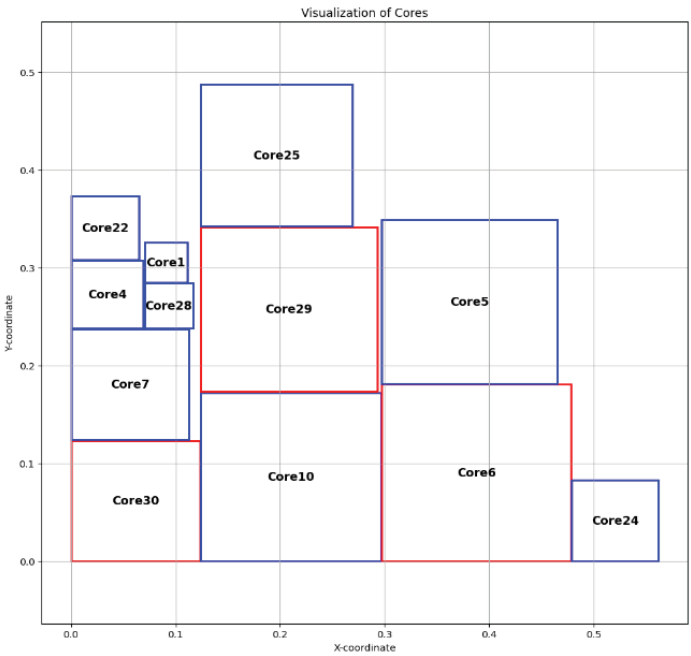

Figure 2: A stack of 3D-SIC with cores from the p93791 SoC

Table 1 provides a comparative analysis of test schedule times for the p93791 3D-SIC, both with and without thermal-aware floor planning. The data clearly demonstrate that the application of thermal-aware floor planning results in shorter test schedule times across various TAM widths. These reductions in the overall test schedule time are attributed to the enhanced heat

dissipation enabled by thermal-aware floor planning. By strategically positioning hot modules away from each other and incorporating non-hot modules as thermal buffers, the system effectively manages heat distribution, which allows more cores to be tested concurrently while keeping the overall temperature of the 3D-SIC within acceptable limits. In contrast, without thermal-aware floor planning, the testing process faces limitations due to increased risk of overheating and the need for more conservative scheduling to avoid thermal issues, thereby resulting in longer test schedule times as fewer cores can be tested concurrently. Hence, this validates the effectiveness of integrating thermal-aware test scheduling with floor planning in optimizing the testing process for complex integrated circuits.

Table 1: Comparison of test time for p93791 3D-SIC

TAM	Test schedule time without floor planning	Test schedule time without floor planning
16	1840033	1803905
24	1209389	1208746
32	1023984	1022562
40	778902	776900
48	648011	646930
56	520930	519883

IV. Conclusion

In conclusion, this paper proposed a co-optimization technique that integrates thermal-aware test scheduling with floor planning for 3D-SICs, effectively addressing challenges related to heat dissipation of 3D-SICs and to minimize total test schedule time, while adhering to power and resource limitations. The method mitigates issues such as hotspot formation from adjacent hot modules and optimizes TSV usage, enabling more cores to be tested concurrently while keeping the overall temperature

within acceptable limits. The objectives were to develop a floor-planning technique that balances power dissipation capability with TAM width and to create a thermal-aware test scheduling method that minimizes test schedule time while adhering to power and resource constraints. The results show that this integrated approach significantly reduces test schedule times and enhances concurrent testing capabilities, outperforming traditional test scheduling techniques that do not consider floor planning. Additionally, integrating more established floor planning techniques with the test scheduling method could enhance heat dissipation and overall system performance. Hence, future research could explore other advanced optimization algorithms, such as Genetic Algorithms or Particle Swarm Optimization, to further improve the integration of floor planning and test scheduling.

V. Acknowledgement

The authors would like to acknowledge that this research was supported by UTM Fundamental Research Grant numbered 22H19.

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